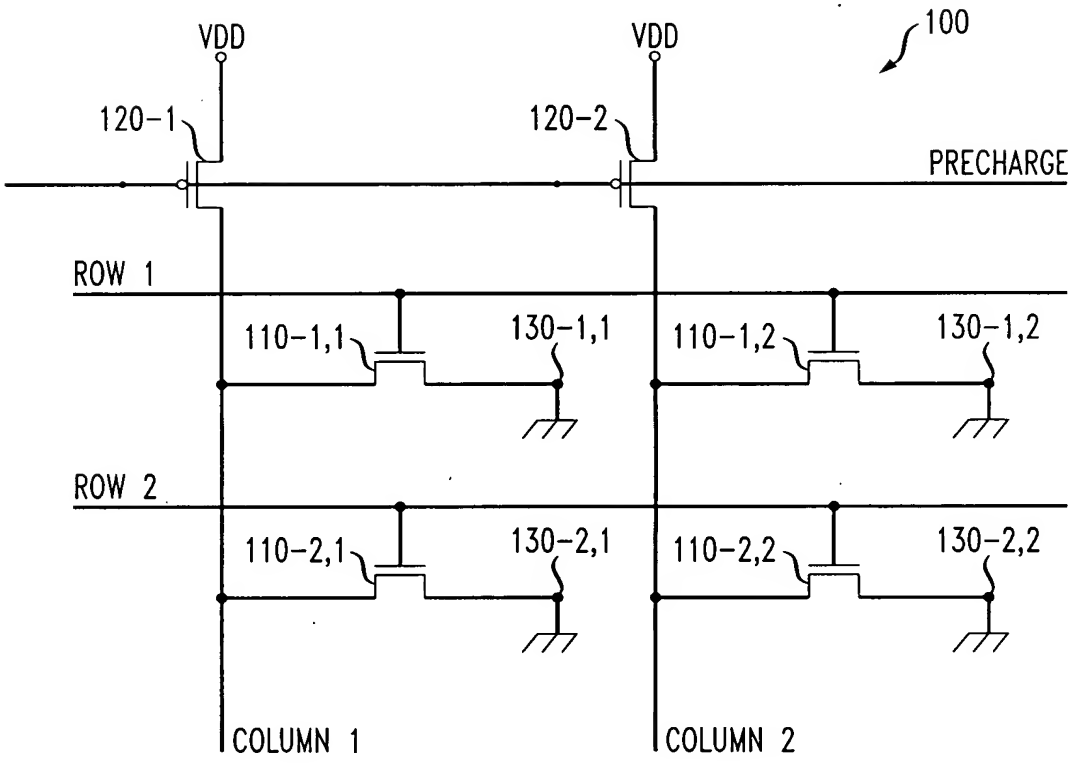
OIPE JC26
MAR 1 0 2004
PATENT & TRADEMARK OFFICE

FIG. 1
PRIOR ART



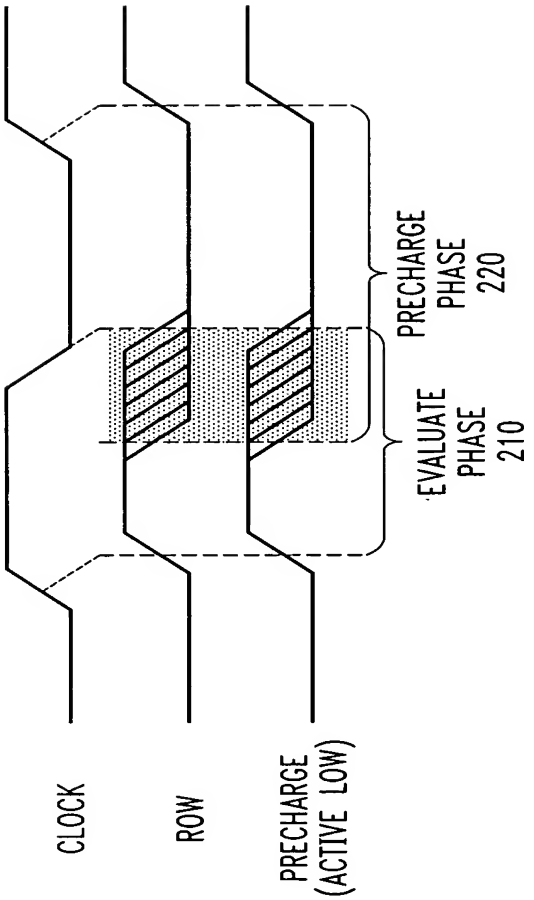


FIG. 2
PRIOR ART

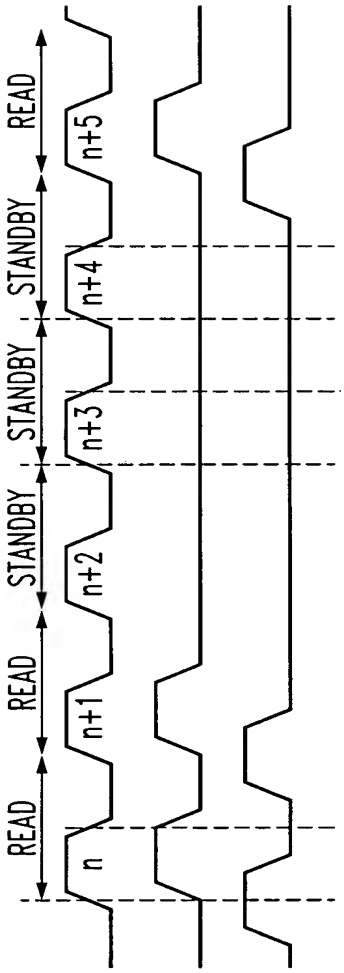


FIG. 3
PRIOR ART

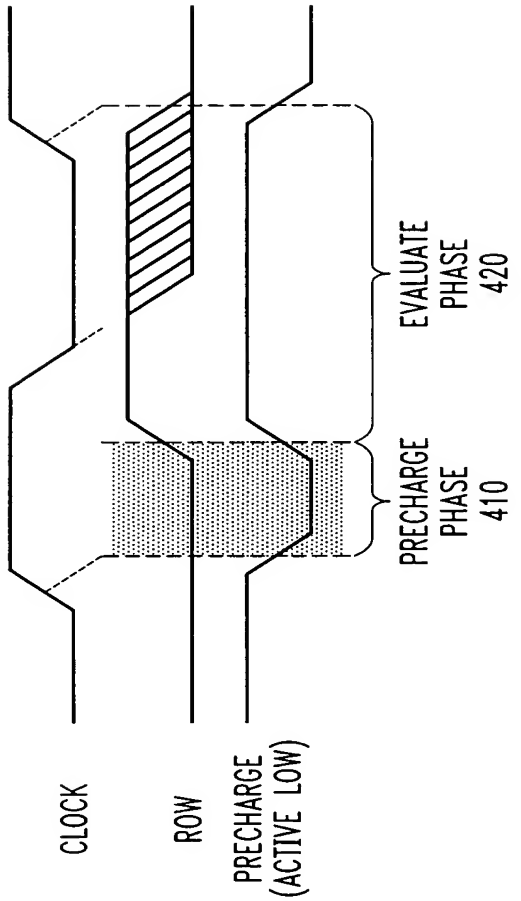

CLOCK
ROW
PRECHARGE (ACTIVE LOW)
PRECHARGE PHASE 410
EVALUATE PHASE 420

FIG. 4

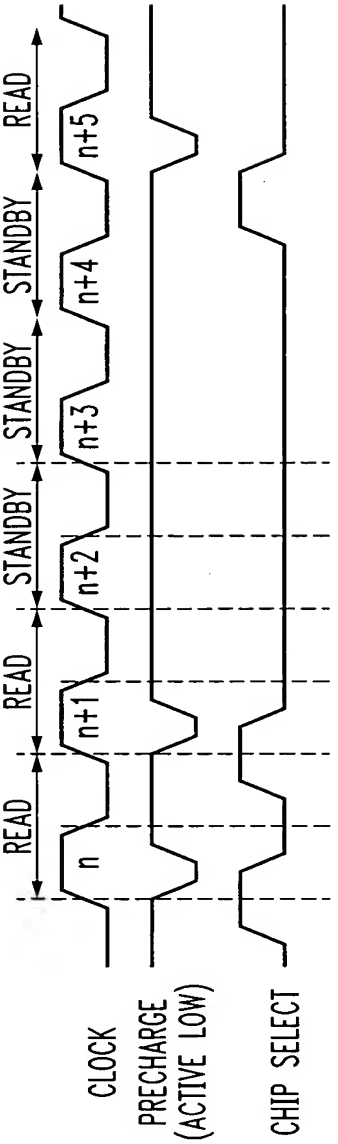

READ
n
READ
n+1
STANDBY
n+2
STANDBY
n+3
STANDBY
n+4
READ
n+5
CLOCK
PRECHARGE (ACTIVE LOW)
CHIP SELECT

FIG. 5

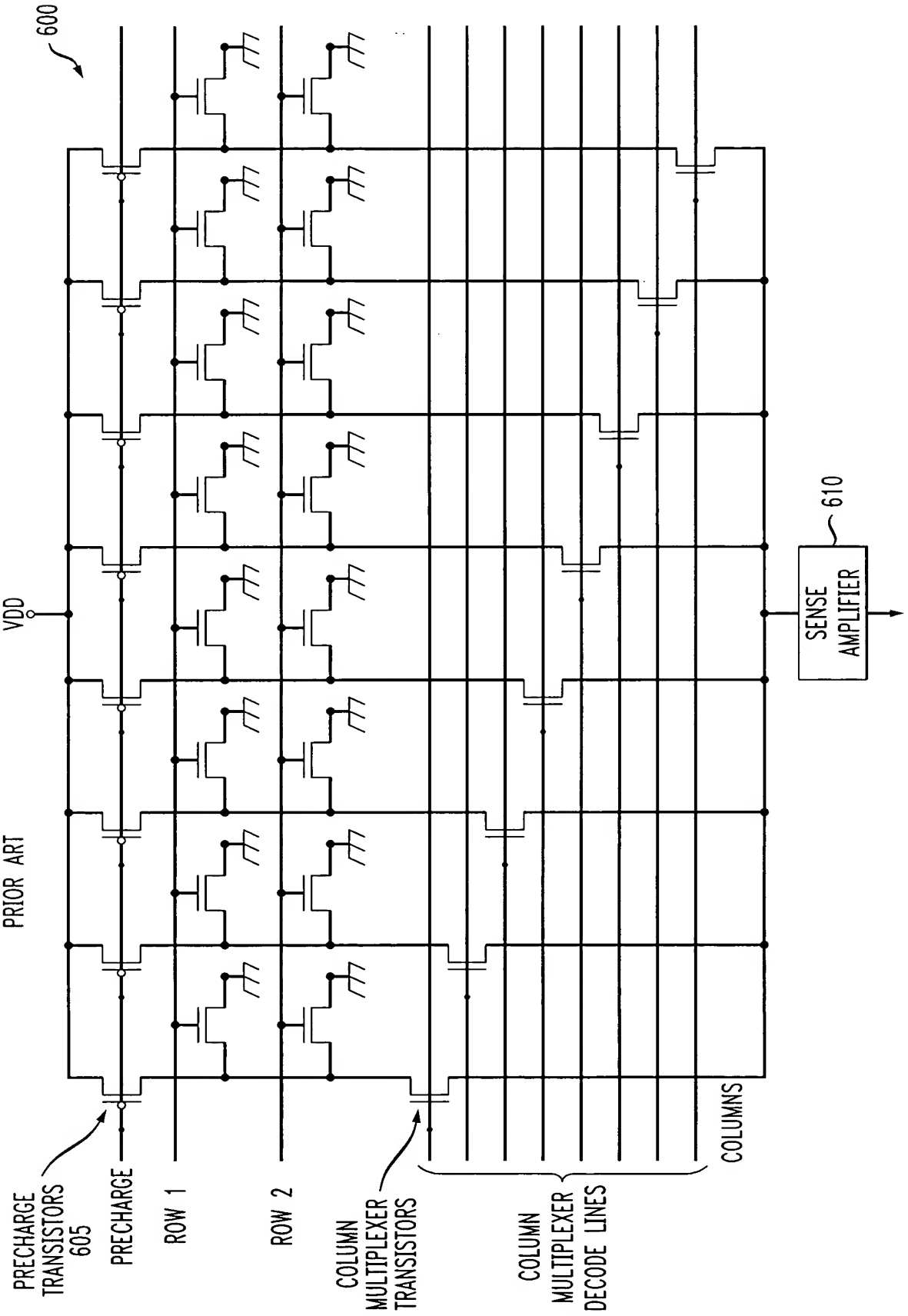


FIG. 6
PRIOR ART

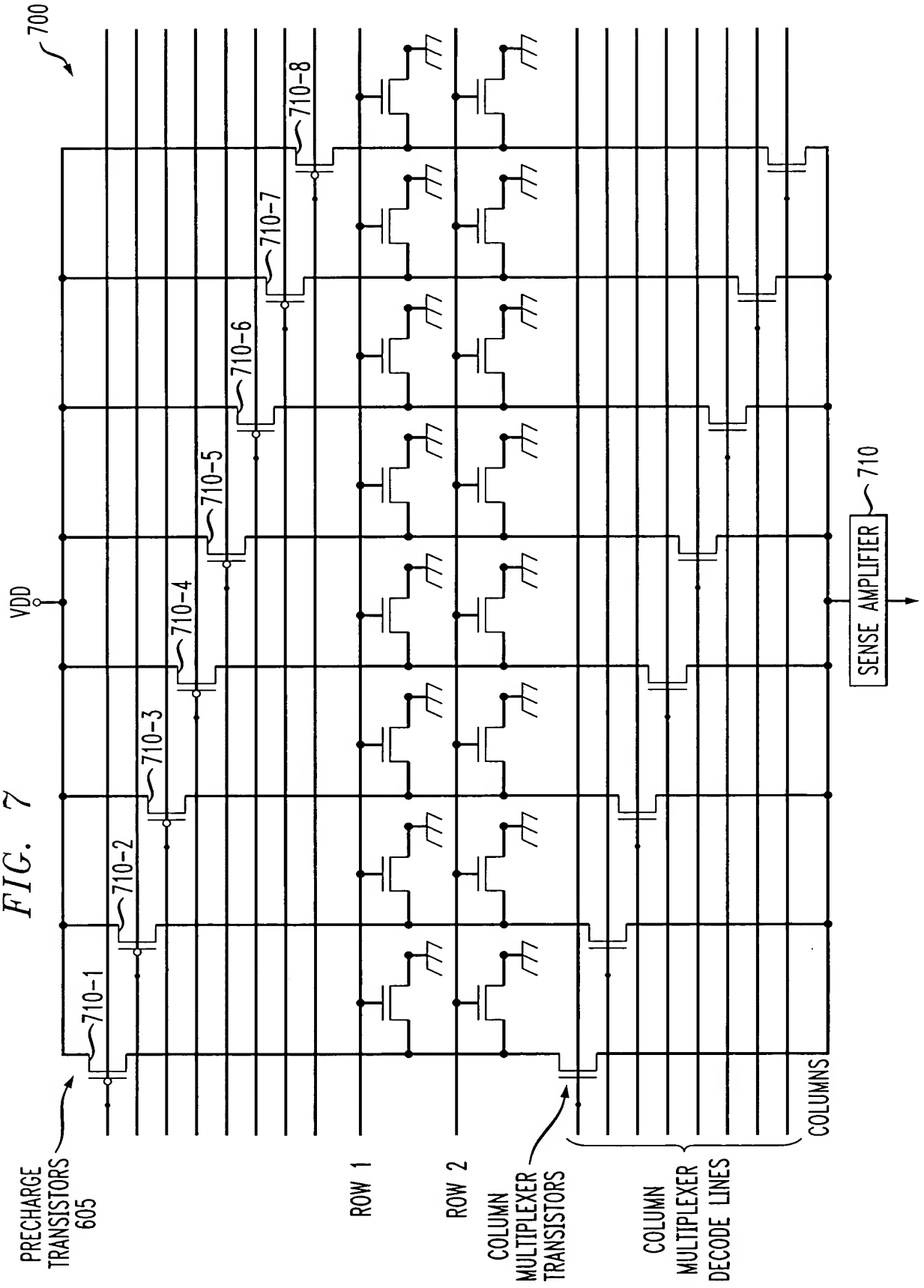

700
710-1
710-2
710-3
710-4
710-5
710-6
710-7
710-8
VDD
710
SENSE AMPLIFIER
PRECHARGE TRANSISTORS 605
ROW 1
ROW 2
COLUMN MULTIPLEXER TRANSISTORS
COLUMN MULTIPLEXER DECODE LINES
COLUMNS

FIG. 7

FIG. 8
PRIOR ART

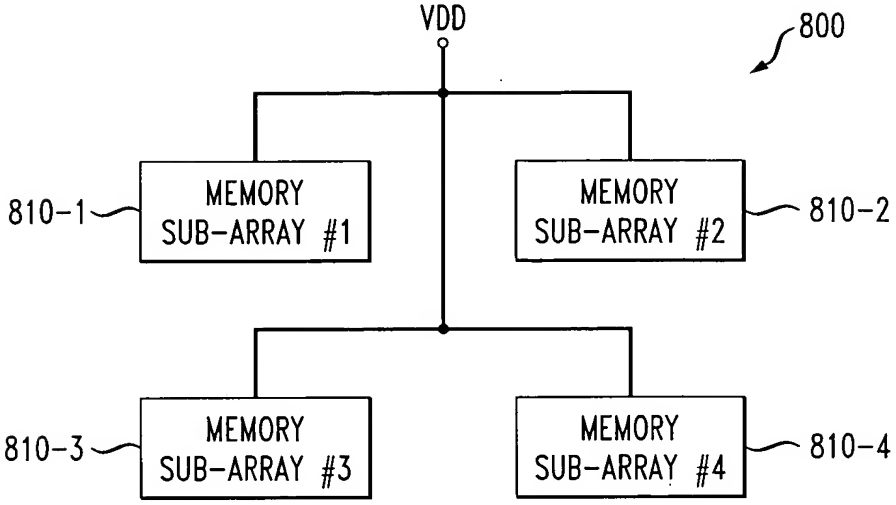
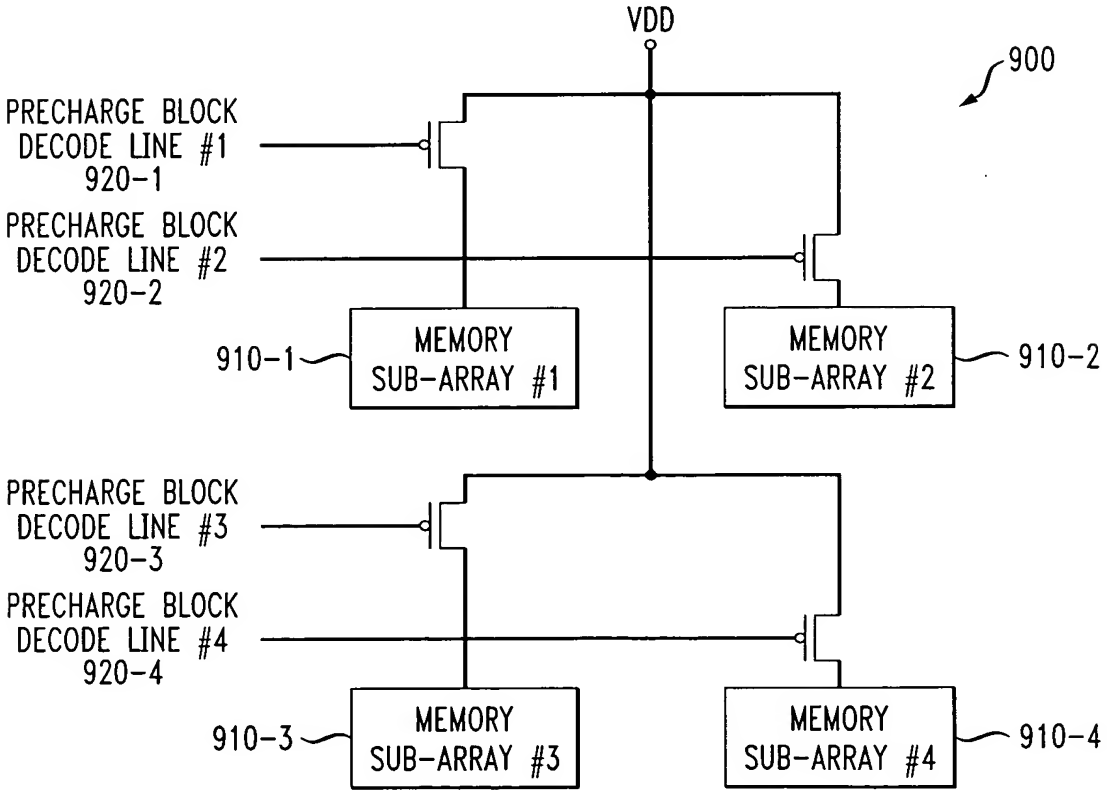



FIG. 9